



⑪ Publication number: **0 605 185 A3**

⑫ **EUROPEAN PATENT APPLICATION**

⑰ Application number: **93310412.7**

⑤① Int. Cl.⁵: **H04N 1/21**

⑱ Date of filing: **22.12.93**

③① Priority: **28.12.92 JP 361631/92**

④③ Date of publication of application: **06.07.94 Bulletin 94/27**

⑥④ Designated Contracting States: **DE FR GB**

⑥⑧ Date of deferred publication of search report: **24.08.94 Bulletin 94/34**

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⑤④ **Image processing apparatus.**

⑤⑦ An image processing apparatus having a solid state image sensor for inputting an optical image thereto and converting the image into an electrical signal; an image memory having a general-purpose DRAM formed by at least one chip and required to control the refresh operation from the outside of the memory chip; a timing signal generator for generating timing of read from the solid state image sensor; a transfer/storage control device for horizontally reading data from the solid state image sensor synchronously with the horizontal read timing signal generated from the timing signal generator, transferring the read data and storing the data in the DRAM; a first refresh signal generator for refreshing the DRAM at predetermined time intervals when no data is read from the solid state image sensor; and a second refresh signal generator for refreshing the DRAM a predetermined number of times during the dormant period of the horizontal read timing signal. In the apparatus, the second refresh signal generator is made effective synchronously with the horizontal read timing signal during the time of read from the solid state image sensor, and the first refresh signal generator is made effective during a time other than the time of read from the solid state image sensor.

